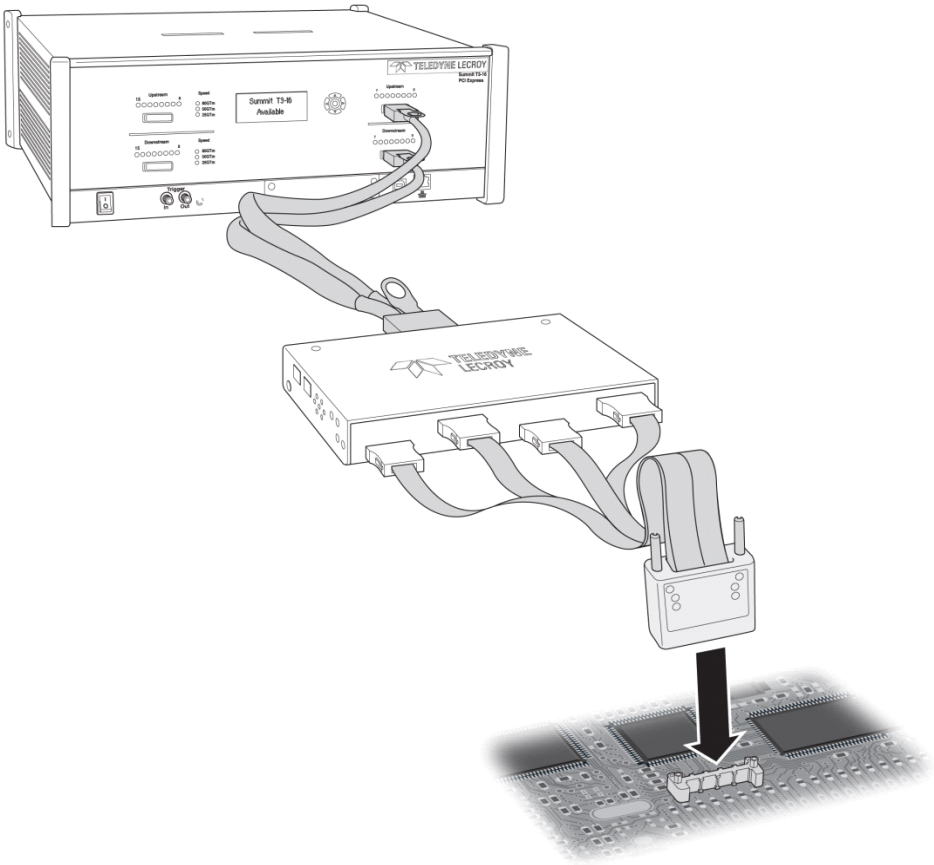
TELEDYNE LECROY
Everywhereyoulook™

PCI Express 3.0 Mid-Bus Probe

Installation and Usage Manual



For use with Summit™ T3-16 / T3-8 / T34 Systems

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Teledyne LeCroy Protocol Solutions Group

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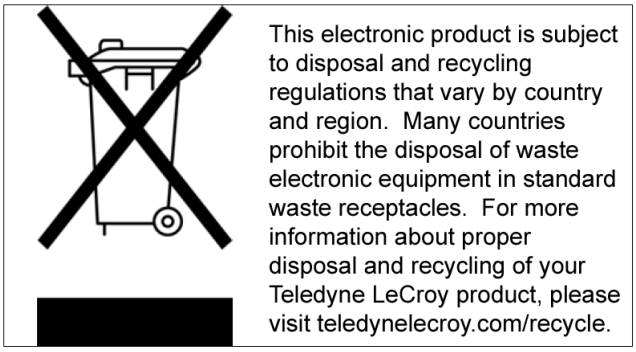
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WEEE Program



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Chapter 1

Introduction

Teledyne LeCroy offers a wide variety of ways to connect PCI Express protocol analyzers to products under test. There are four common methods:

- Interposers
- Specialty Probes
- PCIe Protocol Suite Analyzer Hardware and Software
- Mid-Bus Probes and Multi-lead Probes

1.1 Interposers

If the product uses a standard PCI Express card connector, an interposer is used which is inserted between the PCIe Card and the card slot. The interposer taps off the data traffic to allow the analyzer to monitor and record traffic with minimal perturbation of the electrical interface.

1.2 Specialty Probes

Specialty probes are used with specific card configurations, and are used in the same manner as an interposer card (in fact a specialty probe is an interposer card designed for a specific interface). Teledyne LeCroy supports a range of specialty probes including ExpressCard, AMC, XMC, Mini Card, External Cable, ExpressModule, HP Blade Server and SFF8639 interfaces.

1.3 PCIe Protocol Suite Analyzer Hardware and Software

Designed for developers and validators, the Teledyne LeCroy Summit T3-16™ is a Gen1/ Gen2/Gen3 PCI Express advanced verification system.

By leveraging years of experience in protocol analysis tools for emerging markets, Summit T3-16 blends sophisticated functionality with practical features to speed the development of PCI Express™ IP cores, semiconductors, bridges, switches, add-in boards, and systems.

1.4 Multi-Lead / Mid-Bus Probes

The multi-lead probe allows individual connections to each bus trace on the board. If the product has an embedded PCI Express bus (e.g., a bus which runs between chips on the same circuit board), then either a mid-bus probe or a multi-lead probe can be used. The mid-bus probe requires a connection footprint (see below) to be designed into the board. The Teledyne LeCroy mid-bus probes are 16-channel differential signal probes that meet the demand for high-density signal access, accuracy and repeatability while providing connector-less attachment to the device under test. They are based upon the configuration that was initially recommended in the Intel PCI Express Mid-Bus Probing Footprint and Pinout Revision 1.0 document dated 8/05/03 and the subsequent revisions.

A mid-bus probe is one of the tools that can greatly help engineers debugging PCI Express buses. A PCI Express mid-bus probing solution provides direct probing capability of a PCI Express bus at a width of up to 16 lanes. To accommodate a mid-bus probe, a special pad layout is required to expose the PCI Express differential pairs on the surface of the target board. (See figure below).

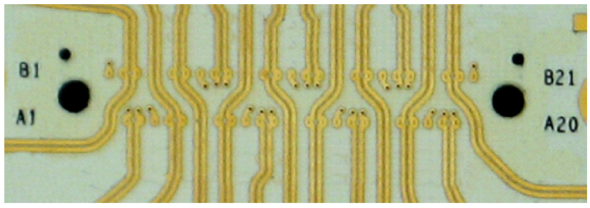


Figure 1.1: Board Trace Layout for a Mid-Bus Probe

Although not part of the PCI Express specifications, the industry has developed common mid-bus probe footprints for PCIe 1.0a, PCIe 2.0 and PCIe 3.0 applications (the "full-size" PCIe 3.0 footprint is shown on the right). These footprints are designed into the PCB. For PCIe 3.0 applications, the probe cable attachment uses a probe connector which is mounted the PCB as shown in the lower image on the below.

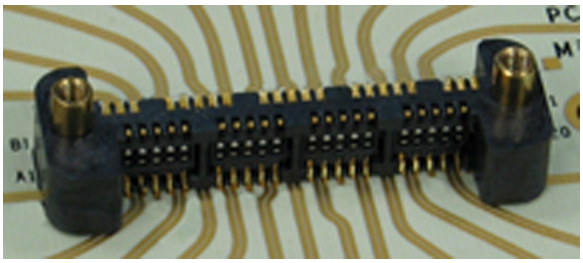


Figure 1.2: Full Width Connector for a Mid-Bus Probe

The appropriate footprint is recommended for use with all types of test equipment including protocol analyzers, logic analyzers and oscilloscopes. The required pad layout can be in x4 (half-size), x8 (full-size) or x16 (dual full-size) configurations depending on the maximum number of lanes that need to be probed. All footprint sizes support probing at reduced lane widths (e.g., x1) and at lane widths up to the maximum footprint size. The illustration Figure 2.1 on page 7 shows the completed assembly for probing up to x8 configurations (for x16 configurations, a second Y-cable, probe pod, header cable

assembly and probe connector are used, but connection is made to the same Summit T3-16 analyzer - see Figure 3.8 on page 15). As noted, a single full-size probe connector supports up to x8 lane widths bidirectional, but can also be configured to support x16 unidirectional (as can a half-size probe connector support x8 unidirectional).

Note: This manual documents the mid-bus footprint used for PCIe 3.0 applications; the probe footprints for PCIe 1.0a and PCIe 2.0 are covered in the Gen2 Mid-Bus Probe User Manual.

Teledyne LeCroy makes two versions of mid-bus probes, one for PCIe 2.0 (2.5 and 5 GT/s data rates, also referred to as "Gen2") and one for PCIe 3.0 (2.5, 5 and 8 GT/s data rates, also referred to as "Gen3"). The PCIe 3.0 mid-bus probe is for use with the Summit T3-16, Summit T3-8, Summit T34 analyzers, and is documented in this manual.

The PCIe 3.0 mid-bus probe, in a similar fashion to the PCIe 1.0a and PCIe 2.0 implementations that preceded it, is available in two versions: a full-size probe and a half-size probe. The full-size probe for is shown on Figure 2.1 on page 7. It has a four-strand ribbon cable and a x16 connection header. A half-size probe has a two strand ribbon cable and a x8 connection header.

The part numbers and components of the Teledyne LeCroy PCIe 3.0 mid-bus probes are as follows:

1.4.1 Complete Kits

1. **PE090ACA-X PCIe 3.0 Mid-Bus Probe Kit***

x8 Lane Width, Full-size Connector, which includes:

- ❑ PE010UCA-X: iPass Y-Cable
- ❑ PE087ACA-X: PCIe 3.0 Mid-Bus Probe Pod with power supply
- ❑ PE057ACA-X: PCIe 3.0 x8 Mid-bus Probe Cable
- ❑ PE009UCA-X: Daisy Chain Clock Cable
- ❑ PE014UCA-X: Reference Clock Cable
- ❑ PE047UIA-X: Gen3 Mid-bus Probe Connector Full-size

* Supports up to x8 bi-directional link or x16 uni-directional link (for use with two Summit T34s, one T3-8 or one T3-16 analyzers).

2. **PE094ACA-X PCIe 3.0 Mid-Bus Probe Kit***

x4 Lane Width, Half-size Connector, which includes:

- ❑ PE010UCA-X: iPass Y-Cable
- ❑ PE087ACA-X: PCIe 3.0 x8 Mid-Bus Pod with power supply
- ❑ PE056ACA-X: Mid-bus Probe Cable (x4)
- ❑ PE009UCA-X: Daisy Chain Clock Cable
- ❑ PE014UCA-X: Reference Clock Cable
- ❑ PE054UIA-X: PCIe 3.0 Mid-bus Probe Connector Half-Size

* Supports up to x4 bi-directional link or x8 uni-directional link (for use with one T3-8 or one T3-16 analyzer).

3. **PE091ACA-X PCIe 3.0 Mid-Bus Probe Kit***

x4 Lane Width, Half-size Connector, which Includes:

- ❑ PE013UCA-X: x4-to-x8 Straight iPass Cable
- ❑ PE087ACA-X: PCIe 3.0 x8 Mid-Bus Pod with power supply
- ❑ PE056ACA-X: Mid-bus Probe Cable (x4)
- ❑ PE009UCA-X: Daisy Chain Clock Cable (second cable for future expandability)
- ❑ PE014UCA-X: Reference Clock Cable (second cable for future expandability)
- ❑ PE054UIA-X: PCIe 3.0 Mid-bus Probe Connector Half-Size

* Supports up to x4 bi-directional link or x8 uni-directional link (for use with one Summit T-34 analyzer only).

TABLE 1.1: Full Size Probe Kit Capabilities

PE090ACA-X PCIe 3.0 x8 Full-Size Probe Kit									
x1		x2		x4		x8		x16	
Uni	Bidir	Uni	Bidir	Uni	Bidir	Uni	Bidir	Uni	Bidir
x	x	x	x	x	x	x	x	x	*

*: For bidirectional x16, two PE090ACA-X kits are required.

TABLE 1.2: Half Size Probe Kit Capabilities

PE094ACA-X / PE091ACA-X PCIe 3.0 x4 Half-Size Probe Kit									
x1		x2		x4		x8		x16	
Uni	Bidir	Uni	Bidir	Uni	Bidir	Uni	Bidir	Uni	Bidir
x	x	x	x	x	x	x			

1.4.2 Individual Components

1. PE087ACA-X PCIe3 Mid-bus Pod with Thumbscrews
   - ❑ No cables (for use with Summit T3-16 or Summit T3-8), includes power supply.
2. PE056ACA-X PCIe3 Mid-bus Probe Cable with Thumbscrews
   - ❑ G3x4 probe cable (Half size -- connects to G3 Mid-bus box, for use with Summit T34, Summit T3-16 or Summit T3-8)
3. PE057ACA-X PCIe3 Mid-bus Probe Cable with Thumbscrews
   - ❑ G3x8 probe cable (Full size -- connects to G3 Mid-bus box, for use with Summit T3-16 or Summit T3-8)
4. PE038UIA-X PCIe Gen3 x8 Dish for Mid-bus Probe
5. PE047UIA-X Gen3 Mid-bus Probe Connector Full-Size

6. PE054UIA-X Gen3 Mid-bus Probe Connector Half-Size
7. PE010UCA-X Y-Cable from Mid-bus Probe Pod to Analyzer
8. PE013UCA-X x4-to-x8 Straight iPass Cable

Chapter 2

Probe Components

2.1 Probe Components

- Y-Cable to Analyzer
- Gen3 Mid-Bus Probe Pod
- Probe Header Cable Assembly
- Probe Connector (mounted to board)
- Clocking Cable* (not shown)

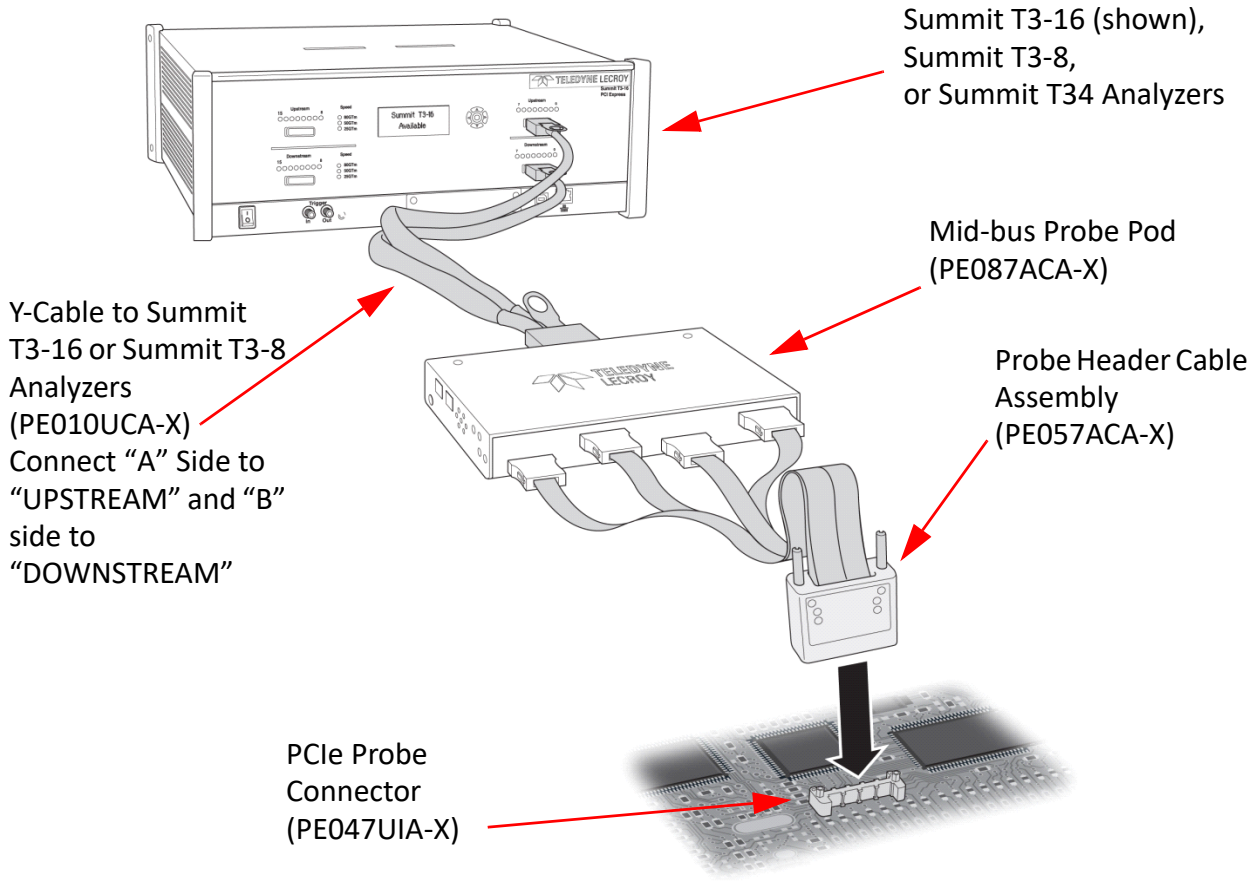


Figure 2.1: Typical Full Size Probe Components

Note: * The Intel-based mid-bus footprint specification only supplies differential lane signaling and ground reference. Should a reference clock (RefClk) be required a separate connection must be made. Teledyne LeCroy PCI Express protocol analyzers can use a reference clock probe in conjunction with the mid-bus analysis. Each mid-bus probe is equipped with one clock probe. The mid-bus reference clock probe is designed to facilitate capturing clock signals from the system board in the two configurations recommended by the Intel guideline, i.e., a tap off of an existing clock or a dedicated clock.

Chapter 3

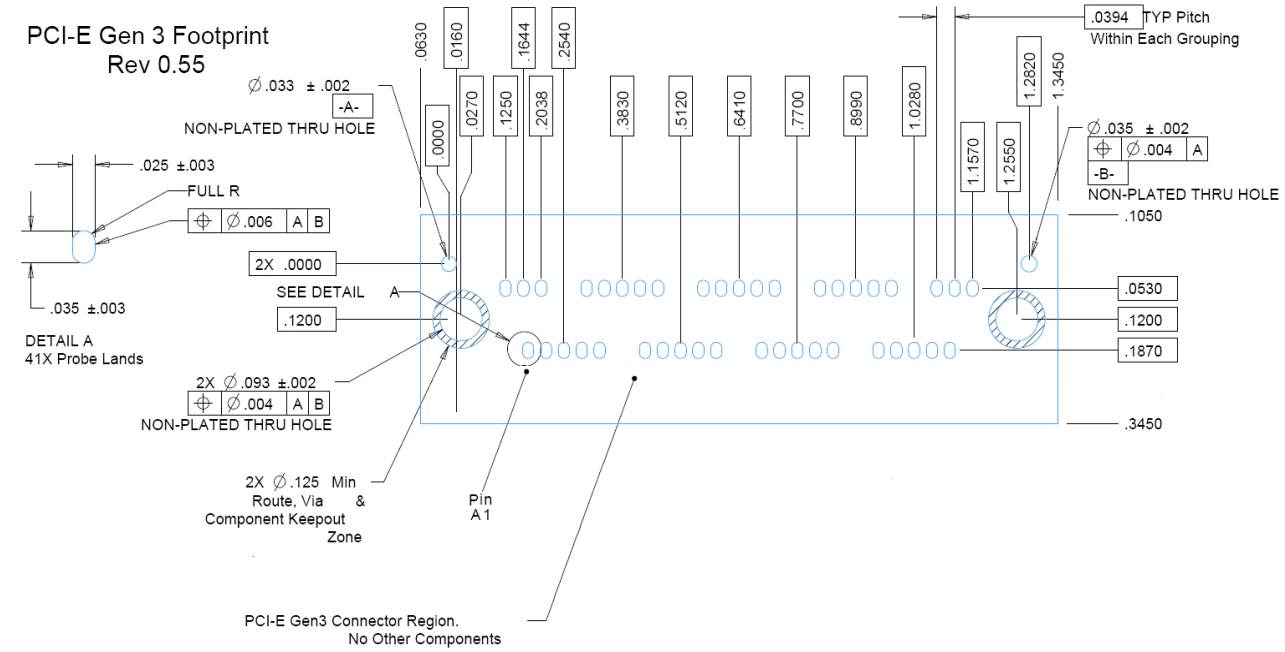
Mechanical Design

This section describes footprint dimensions, keepout volumes, and probe pin assignments.

3.1 Probe Footprints

The Mid-bus Probe is fully compatible with the standardized mid-bus footprint recommended by the Intel guideline, as shown in the following figures.

Full-Size Probe Footprint



Notes:
1) All Dims INCHES
2) Soldermask openings associated with probe lands must be no smaller than probe lands. Solder mask must not encroach on pad region.
3) Via placement in pads is not allowed unless the vias are filled, planarized, and plated as specified in note 5.
4) Refer to KOV drawing for detail regarding keepout height and volume and secondary side constraints.
5) Plating of pads needs to be coplanar, low contact resistance, and not subject to corrosion/degradation. ENIG surface finish is recommended to satisfy these requirements. The pads must be protected from solder during assembly operations to maintain the gold finish. The following PCB flag note is suggested:

Surface finish shall be 3-7 microinches of immersion gold over 50-150 micro inches of electroless nickel.

Figure 3.1: PCIe Gen 3 Footprint

PCIe Gen 3 Full Size Keepout Volume

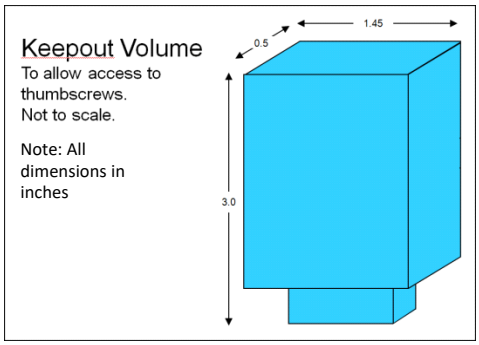
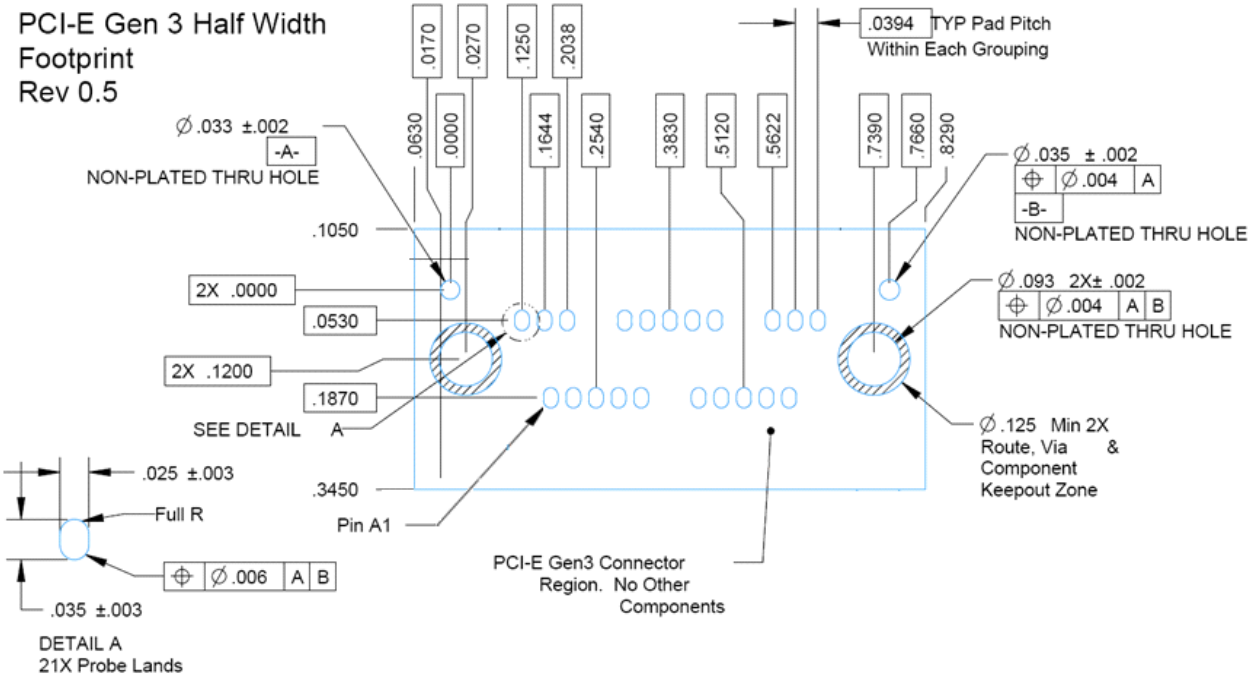


Figure 3.2: PCIe Gen 3 Keepout Volume

Half-Size Probe Footprint



Notes:
1) All Dims INCHES
2) Soldermask openings associated with probe lands must be no smaller than probe lands. Solder mask must not encroach on pad region.
3) Via placement in pads is not allowed unless the vias are filled, planarized, and plated as specified in note 5.
4) Refer to KOV drawing for detail regarding keepout height and volume and secondary side constraints.
5) Plating of pads needs to be coplanar, low contact resistance, and not subject to corrosion/degradation. ENIG surface finish is recommended to satisfy these requirements. The pads must be protected from solder during assembly operations to maintain the gold finish. The following PCB flag note is suggested:

Surface finish shall be 3-7 microinches of immersion gold over 50-150 micro inches of electroless nickel.

Figure 3.3: PCIe Gen 3 Half Width Footprint

PCIe Gen 3 Half Size Keepout Volume

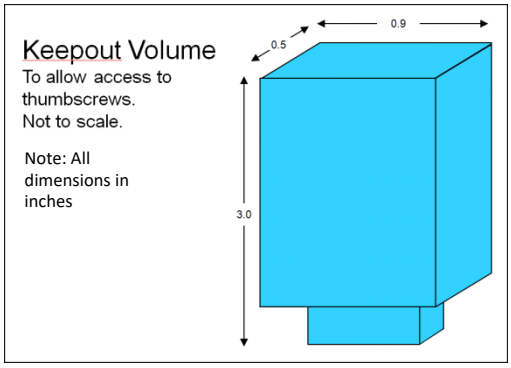


Figure 3.4: PCIe Gen 3 Half Width Probe Keepout Volume

PCB Layout of Full Size PCIe Gen 3 Mid-bus Footprint

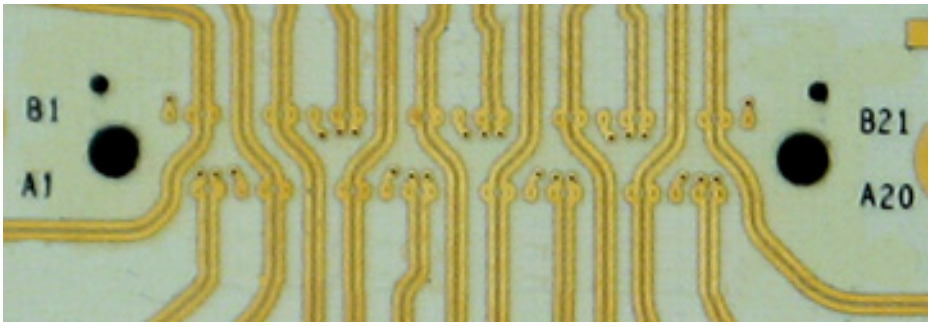


Figure 3.5: Full Size PCIe Gen 3 PCB Footprint

PCB Layout of Half Size PCIe Gen 3 Mid-bus Footprint

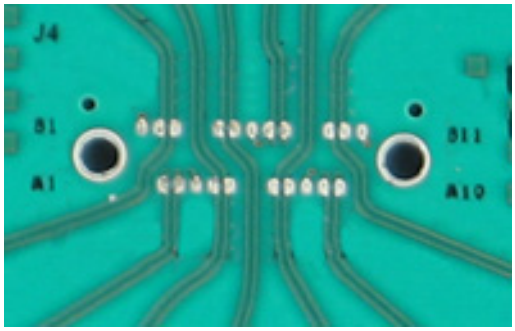


Figure 3.6: Half Size PCIe Gen 3 PCB Footprint

3.2 Mid-bus Probe Retention

To prepare a circuit board for PCI Express mid-bus probing, the mid-bus footprint has to be laid out onto the target system board and a probe connector has to be attached to the board. Attachment of the probe connector is simple and quick. There are two through-hole screws and one protrusion key underneath the probe connector. Align the key of the probe connector with the keying/alignment hole in the mid-bus footprint on the target system board, and connect the small screws (supplied) through the PCB and into the threaded holes on the underside of the Mid-bus connector module, and tighten the screws to ensure good contact between the contacts of the connector and the pads on

the PCB. The mid-bus probe can then be attached to the target system board through the probe connector to provide mechanical support for pin-to-pin alignment. The mid-bus cable has 2 retention screws that connect to the probe connector to hold the probe in place.

Cable to PCB Connector



Figure 3.7: Cable Connection to PCB Connector

Note: The attachment screws supplied will provide secure attachment for most PCB designs. If the PCB is very thick, the screws may not be long enough to pass through the PCB and securely attach the Mid-bus connector module, in which cases longer screws will be needed. The screws supplied are 5mm long (McMaster-Carr P/N 91292A005), and longer lengths can be obtained directly from McMaster-Carr in 6mm (91292A006), 8mm (91292A008), or longer lengths as needed.

The probe connector should not be confused with a PCB connector because it is not part of the electrical circuits of either the target system or the probe.

PCIe 3.0 probe connectors can be purchased through Teledyne LeCroy:

- **Full-size: P/N PE047UIA-X**
- **Half-size: P/N PE054UIA-X**

3.3 Probe Connection to Analyzer

The bus signals captured by the mid-bus probe are connected to a mid-bus probe pod for amplification. This reduces the load imposed by the mid-bus probe on the target system, while allowing a longer cable to attach to the Teledyne LeCroy PCI Express protocol analyzer. The Teledyne LeCroy PCI Express protocol analyzer can then interpret these signals for full decoding and protocol analysis.

3.4 Probe Keepout Volume

As with any connection to a PCB, sufficient clearance must be allowed around the point where the probe will connect. This is defined as the keep-out volume, which must be kept clear of other components mounted on the PCB.

The probe keepout volumes are shown in the diagrams in "Probe Footprints" on page 9.

3.5 Reference Clock Probe Attachment

Should SSC clocking be used in the system under test or if the link varies the bit rate by more than 100 MHz ± 300ppm (see Section 4.3.7 of Base Spec 3.0), a reference clock tap may be required. The connection from the reference clock to the analyzer is a 3-pin header (1 by 3, 0.050" center spacing) which is placed on the clock signal transmission line of the DUT. The PE014UCA-X Reference Clock Cable provides a three-pin micro socket that connects from this header to the CLK IN port on the Mid-Bus Pod.

If the reference clock is sampled by tapping off an existing clock, the header shall be located on the existing clock transmission line, where a high impedance clock probe from the mid-bus probe is connected with no significant loading effects. In the case of a dedicated clock, the header shall be located at the end of a dedicated clock transmission line without termination, where a 50-Ohm cable is connected and the termination for the clock signal is provided on the mid-bus probe board.

The connectivity of the clock header pins follows the following table:

TABLE 3.3: Clock Header Pins

Signal	Pin Number
REFCLKp	1 (or 3)
Unused	2
REFCLKn	3 (or 1)

Note: The analyzer is not sensitive to the polarity of the reference clock. Therefore, the probe can be plugged onto the pin header in either orientation.

The following 3-pin header can be used for the reference clock:

- Samtec Part No: TMS-103 (Vertical Orientation)

The reference clock is captured separately with a dedicated probe cable. Considering the possibility that one clock may be shared between two physically separated mid-bus probes, each mid-bus probe pod is equipped with a reference clock output port. The reference clock probe can capture signals from the target system or receive a duplicated reference clock from another mid-bus probe board.

3.6 Daisy Chain Cable (for x16 applications)

A single mid-bus probe pod can capture traffic on bus widths up to x8. If x16 lane widths are required (e.g., when using a Summit T3-16 Analyzer with a x16 device), two Mid-Bus Probe Pods are required.

In this configuration, one of the pods is connected to the DUT to tap the Reference Clock signal, and the second pod is "daisy-chained" to the first pod using the PE009UCA-X Daisy Chain Cable. Connect the Ref Clock cable to the **CLK IN** port of the first pod, and connect the Daisy Chain Cable between the **CLK OUT** port of the first pod and the **CLK IN** port of the second pod.

Mid-bus Probe Setup for x16 lane widths
(using Summit T3-16 Analyzer, Clocking Cable not shown)

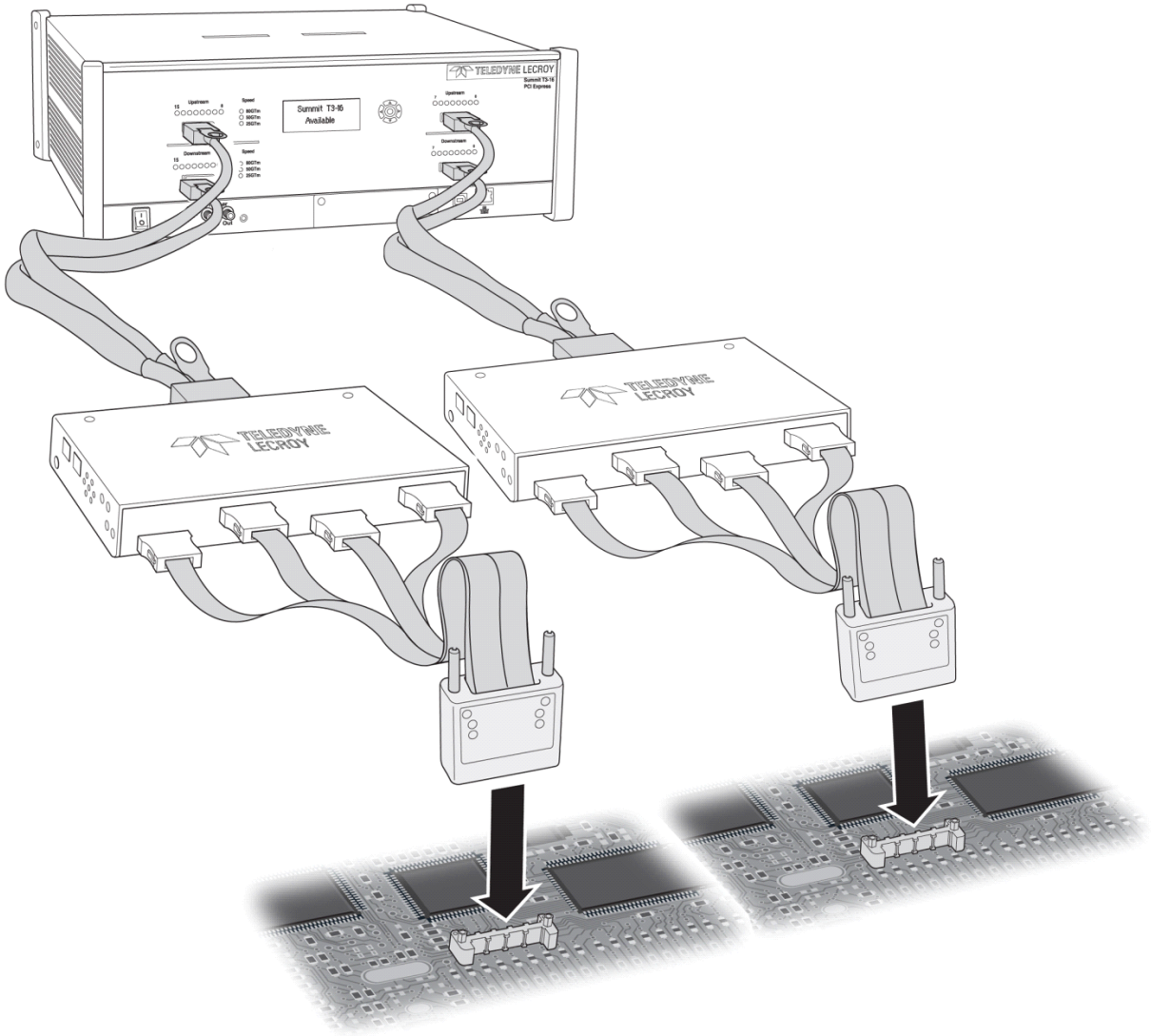


Figure 3.8: Mid-bus Probe Setup for x16 lane widths

Chapter 4

Electrical Design

4.1 Probe Loading Effect

The logical probing of the PCI Express bus is achieved by tapping a small amount of energy from the probed signals and channeling this energy to the analyzer. To avoid excessive loading conditions, the Teledyne LeCroy mid-bus probe employs high impedance tip resistors (isolation resistors). The probe isolation resistance is selected to both satisfy the probe sensitivity and system parasitic load requirements.

Extensive care has been taken to reduce the parasitic effect of the probed signals during each phase of the mid-bus probe design. The equivalent load model of the Mid-bus probe is available in HSPICE parameters. It is an empirical-based model that involves complicated connectivity. It can be requested from the Teledyne LeCroy Protocol Systems Group support team (psgsupport@teledynelecroy.com)

With this unique design, the Teledyne LeCroy mid-bus probes can capture bus traffic signals with amplitudes specified by the PCI Express standard, while introducing only slight loss and jitter on the channel under test. To determine the exact numbers, customers are encourage to simulate their channel using Teledyne LeCroy's model.

4.2 Probed Signal Electrical Requirements

The probe requires the following minimum differential signal requirements at a given bit error rate at the analyzer probe point:

- Inner eye width = 82 ps Minimum (see 1 in the following figure)
- Inner eye height = 52 mVpp Minimum (see 2 in the following figure)
- Maximum signal amplitude 1500 mVpp Maximum (see 3 in the following figure)

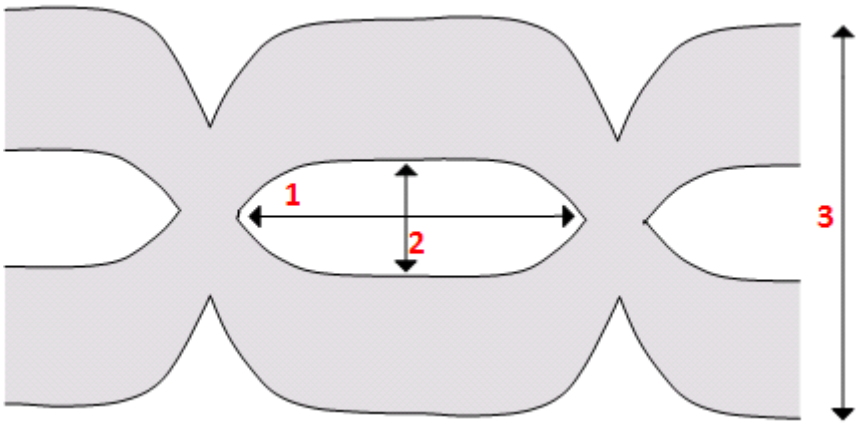


Figure 4.9: Signal Requirements for MidBus Probe

4.3 Overview of Probe - Pin Assignments

Cross-references from the *PCI Express Mid-Bus Probing Footprint and Pinout* (8/05/03) Revision 1.0 are given in tables listed below.

The Summit T3-16 PCI Express analyzers from Teledyne LeCroy support a lane swizzling feature which allows pairs of differential pin assignments to be re-wired dynamically to match the configuration under the probe. This also provides additional versatility in the case where two busses are mapped to the probe footprint and cannot be uniquely positioned within a quadrant. Lane swizzling allow you to reorder upstream lanes or recorder downstream lanes regardless of the order of physical connections – however, you cannot interchange upstream lanes with downstream lanes.

In the pinout tables that follow, the following variations may be applied:

- The designation of upstream and downstream may be reversed as long as it is reversed for every lane (all upstream connections on the left and all downstream on the right may be swapped).
- Lane ordering may be reversed if done as a whole such that probe lanes 0, 1, 2, 3, 4, 5, 6, 7 connect to physical lanes 7, 6, 5, 4, 3, 2, 1, 0.

Note: The Summit T3-16 analyzer provides the flexibility to reorder lanes regardless of the order in which they are physically connected (lane swizzling).

- Each differential signal pair may have the D+ and D- assignment reversed.

4.4 Pin Assignments for Full-size Probe Connectors

For x16 lane widths, two full-size headers are required. The diagrams below show the recommended pin assignments for x16 configurations (keep in mind that any of modifications mentioned in Overview of Probe - Pin Assignments can be applied, and in addition the lane swizzling feature of the Summit T3-16 system noted in “Overview of Probe - Pin Assignments” on page 18).

TABLE 4.4: Table Legend For All Pinout Tables

Character	Function
C	Channel
Ln	Lane
U	Upstream
D	Downstream
p	Positive Polarity
n	Negative polarity

TABLE 4.5: General 16 Channel PCIe Pinout

Pin #	Signal Name	Pin #	Signal Name
		B1	GND
A1	C1p	B2	C0p
A2	C1n	B3	C0n
A3	GND		
A4	C2p	B4	C3p
A5	C2n	B5	C3n
		B6	GND
A6	C5p	B7	C4p
A7	C5n	B8	C4n
A8	GND		
A9	C6p	B9	C7p
A10	C6n	B10	C7n
		B11	GND
A11	C9p	B12	C8p
A12	C9n	B13	C8n
A13	GND		
A14	C10p	B14	C11p
A15	C10n	B15	C11n
		B16	GND
A16	C13p	B17	C12p
A17	C13n	B18	C12n
A18	GND		
A18	C14p	B19	C15p
A20	C14n	B20	C15n
		B21	GND

TABLE 4.6: x16 (One Uni-Directional) Specific 16 Channel PCIe Pinout

Pin #	Signal Name	Pin #	Signal Name
		B1	GND
A1	Ln1p	B2	Ln0p
A2	Ln1n	B3	Ln0n
A3	GND		
A4	Ln2p	B4	Ln3p
A5	Ln2n	B5	Ln3n
		B6	GND
A6	Ln5p	B7	Ln4p
A7	Ln5n	B8	Ln4n
A8	GND		
A9	Ln6p	B9	Ln7p
A10	Ln6n	B10	Ln7n
		B11	GND
A11	Ln9p	B12	Ln8p
A12	Ln9n	B13	Ln8n
A13	GND		
A14	Ln10p	B14	Ln11p
A15	Ln10n	B15	Ln11n
		B16	GND
A16	Ln13p	B17	Ln12p
A17	Ln13n	B18	Ln12n
A18	GND		
A18	Ln14p	B19	Ln15p
A20	Ln14n	B20	Ln15n
		B21	GND

TABLE 4.7: x8 (One Bi-Directional) Specific 16 Channel PCIe Pinout

Pin #	Signal Name	Pin #	Signal Name
		B1	GND
A1	Ln0p-D	B2	Ln0p-U
A2	Ln0n-D	B3	Ln0n-U
A3	GND		
A4	Ln1p-D	B4	Ln1p-U
A5	Ln1n-D	B5	Ln1n-U
		B6	GND
A6	Ln2p-D	B7	Ln2p-U
A7	Ln2n-D	B8	Ln2n-U
A8	GND		
A9	Ln3p-D	B9	Ln3p-U
A10	Ln3n-D	B10	Ln3n-U
		B11	GND
A11	Ln4p-D	B12	Ln4p-U
A12	Ln4n-D	B13	Ln4n-U
A13	GND		
A14	Ln5p-D	B14	Ln5p-U
A15	Ln5n-D	B15	Ln5n-U
		B16	GND
A16	Ln6p-D	B17	Ln6p-U
A17	Ln6n-D	B18	Ln6n-U
A18	GND		
A18	Ln7p-D	B19	Ln7p-U
A20	Ln7n-D	B20	Ln7n-U
		B21	GND

TABLE 4.8: x8 (Two Uni-Directional) Specific 16 Channel PCIe Pinout

Pin #	Signal Name	Pin #	Signal Name
		B1	GND
A1	Ln1p-1	B2	Ln0p-1
A2	Ln1n-1	B3	Ln0n-1
A3	GND		
A4	Ln2p-1	B4	Ln3p-1
A5	Ln2n-1	B5	Ln3n-1
		B6	GND
A6	Ln5p-1	B7	Ln4p-1
A7	Ln5n-1	B8	Ln4p-1
A8	GND		
A9	Ln6p-1	B9	Ln7p-1
A10	Ln6n-1	B10	Ln7n-1
		B11	GND
A11	Ln1p-2	B12	Ln0p-2
A12	Ln1n-2	B13	Ln0n-2
A13	GND		
A14	Ln2p-2	B14	Ln3p-2
A15	Ln2n-2	B15	Ln3n-2
		B16	GND
A16	Ln5p-2	B17	Ln4p-2
A17	Ln5n-2	B18	Ln4n-2
A18	GND		
A18	Ln6p-2	B19	Ln7p-2
A20	Ln6n-2	B20	Ln7n-2
		B21	GND

TABLE 4.9: x4 (Two Bi-Directional) Specific 16 Channel PCIe Pinout

Pin #	Signal Name	Pin #	Signal Name
		B1	GND
A1	Ln0p-D1	B2	Ln0p-U1
A2	Ln0n-D1	B3	Ln0n-U1
A3	GND		
A4	Ln1p-D1	B4	Ln1p-U1
A5	Ln1n-D1	B5	Ln1n-U1
		B6	GND
A6	Ln2p-D1	B7	Ln2p-U1
A7	Ln2n-D1	B8	Ln2p-U1
A8	GND		
A9	Ln3p-D1	B9	Ln3p-U1
A10	Ln3n-D1	B10	Ln3n-U1
		B11	GND
A11	Ln0p-D2	B12	Ln0p-U2
A12	Ln0n-D2	B13	Ln0n-U2
A13	GND		
A14	Ln1p-D2	B14	Ln1p-U2
A15	Ln1n-D2	B15	Ln1n-U2
		B16	GND
A16	Ln2p-D2	B17	Ln2p-U2
A17	Ln2n-D2	B18	Ln2n-U2
A18	GND		
A18	Ln3p-D2	B19	Ln3p-U2
A20	Ln3n-D2	B20	Ln3n-U2
		B21	GND

TABLE 4.10: x4 (Four Uni-Directional) Specific 16 Channel PCIe Pinout

Pin #	Signal Name	Pin #	Signal Name
		B1	GND
A1	Ln1p-1	B2	Ln0p-1
A2	Ln1n-1	B3	Ln0n-1
A3	GND		
A4	Ln2p-1	B4	Ln3p-1
A5	Ln2n-1	B5	Ln3n-1
		B6	GND
A6	Ln1p-2	B7	Ln0p-2
A7	Ln1n-2	B8	Ln0p-2
A8	GND		
A9	Ln2p-2	B9	Ln3p-2
A10	Ln2n-2	B10	Ln3n-2
		B11	GND
A11	Ln1p-3	B12	Ln0p-3
A12	Ln1n-3	B13	Ln0n-3
A13	GND		
A14	Ln2p-3	B14	Ln3p-3
A15	Ln2n-3	B15	Ln3n-3
		B16	GND
A16	Ln1p-4	B17	Ln0p-4
A17	Ln1n-4	B18	Ln0n-4
A18	GND		
A18	Ln2p-4	B19	Ln3p-4
A20	Ln2n-4	B20	Ln3n-4
		B21	GND

TABLE 4.11: x4 (Two Uni-Directional) Specific 16 Channel PCIe Pinout

Pin #	Signal Name	Pin #	Signal Name
		B1	GND
A1	Ln1p-1	B2	Ln0p-1
A2	Ln1n-1	B3	Ln0n-1
A3	GND		
A4	Ln2p-1	B4	Ln3p-1
A5	Ln2n-1	B5	Ln3n-1
		B6	GND
A6	NC	B7	NC
A7	NC	B8	NC
A8	GND		
A9	NC	B9	NC
A10	NC	B10	NC
		B11	GND
A11	Ln1p-2	B12	Ln0p-2
A12	Ln1n-2	B13	Ln0n-2
A13	GND		
A14	Ln2p-2	B14	Ln3p-2
A15	Ln2n-2	B15	Ln3n-2
		B16	GND
A16	NC	B17	NC
A17	NC	B18	NC
A18	GND		
A18	NC	B19	NC
A20	NC	B20	NC
		B21	GND

TABLE 4.12: x2 (Two Bi-Directional) Specific 16 Channel PCIe Pinout

Pin #	Signal Name	Pin #	Signal Name
		B1	GND
A1	Ln0p-D1	B2	Ln0p-U1
A2	Ln0n-D1	B3	Ln0n-U1
A3	GND		
A4	Ln1p-D1	B4	Ln1p-U1
A5	Ln1n-D1	B5	Ln1n-U1
		B6	GND
A6	NC	B7	NC
A7	NC	B8	NC
A8	GND		
A9	NC	B9	NC
A10	NC	B10	NC
		B11	GND
A11	Ln0p-D2	B12	Ln0p-U2
A12	Ln0n-D2	B13	Ln0n-U2
A13	GND		
A14	Ln1p-D2	B14	Ln1p-U2
A15	Ln1n-D2	B15	Ln1n-U2
		B16	GND
A16	NC	B17	NC
A17	NC	B18	NC
A18	GND		
A18	NC	B19	NC
A20	NC	B20	NC
		B21	GND

TABLE 4.13: x2 (Four Uni-Directional) Specific 16 Channel PCIe Pinout

Pin #	Signal Name	Pin #	Signal Name
		B1	GND
A1	Ln1p-1	B2	Ln0p-1
A2	Ln1n-1	B3	Ln0n-1
A3	GND		
A4	NC	B4	NC
A5	NC	B5	NC
		B6	GND
A6	Ln1p-2	B7	Ln0p-2
A7	Ln1n-2	B8	Ln0n-2
A8	GND		
A9	NC	B9	NC
A10	NC	B10	NC
		B11	GND
A11	Ln1p-3	B12	Ln0p-3
A12	Ln1n-3	B13	Ln0n-3
A13	GND		
A14	NC	B14	NC
A15	NC	B15	NC
		B16	GND
A16	Ln1p-4	B17	Ln0p-4
A17	Ln1n-4	B18	Ln0n-4
A18	GND		
A18	NC	B19	NC
A20	NC	B20	NC
		B21	GND

TABLE 4.14: x1 (Two Bi-Directional) Specific 16 Channel PCIe Pinout

Pin #	Signal Name	Pin #	Signal Name
		B1	GND
A1	Ln0p-D1	B2	Ln0p-U1
A2	Ln0n-D1	B3	Ln0n-U1
A3	GND		
A4	NC	B4	NC
A5	NC	B5	NC
		B6	GND
A6	NC	B7	NC
A7	NC	B8	NC
A8	GND		
A9	NC	B9	NC
A10	NC	B10	NC
		B11	GND
A11	Ln0p-D2	B12	Ln0p-U2
A12	Ln0n-D2	B13	Ln0n-U2
A13	GND		
A14	NC	B14	NC
A15	NC	B15	NC
		B16	GND
A16	NC	B17	NC
A17	NC	B18	NC
A18	GND		
A18	NC	B19	NC
A20	NC	B20	NC
		B21	GND

TABLE 4.15: x1 (Four Uni-Directional) Specific 16 Channel PCIe Pinout

Pin #	Signal Name	Pin #	Signal Name
		B1	GND
A1	NC	B2	Ln0p-1
A2	NC	B3	Ln0n-1
A3	GND		
A4	NC	B4	NC
A5	NC	B5	NC
		B6	GND
A6	NC	B7	Ln0p-2
A7	NC	B8	Ln0n-2
A8	GND		
A9	NC	B9	NC
A10	NC	B10	NC
		B11	GND
A11	NC	B12	Ln0p-3
A12	NC	B13	Ln0n-3
A13	GND		
A14	NC	B14	NC
A15	NC	B15	NC
		B16	GND
A16	NC	B17	Ln0p-4
A17	NC	B18	Ln0n-4
A18	GND		
A18	NC	B19	NC
A20	NC	B20	NC
		B21	GND

4.5 Pin Assignments for Half-Size Probe Connectors

TABLE 4.16: Table Legend for all Half-Size Probe Connectors

Character	Function
C	Channel
Ln	Lane
U	Upstream
D	Downstream
p	Positive Polarity
n	Negative polarity

TABLE 4.17: General 8 Channel PCIe Gen3 Pinout

Pin #	Signal Name	Pin #	Signal Name
		B1	GND
A1	C1p	B2	C0p
A2	C1n	B3	C0n
A3	GND		
A4	C2p	B4	C3p
A5	C2n	B5	C3n
		B6	GND
A6	C5p	B7	C4p
A7	C5n	B8	C4n
A8	GND		
A9	C6p	B9	C7p
A10	C6n	B10	C7n
		B11	GND

TABLE 4.18: x8 (One Uni-Directional) Specific 8 Channel PCIe Pinout

Pin #	Signal Name	Pin #	Signal Name
		B1	GND
A1	Ln1p-1	B2	Ln0p-1
A2	Ln1n-1	B3	Ln0n-1
A3	GND		
A4	Ln2p-1	B4	Ln3p-1
A5	Ln2n-1	B5	Ln3n-1
		B6	GND
A6	Ln5p-1	B7	Ln4p-1
A7	Ln5n-1	B8	Ln4n-1
A8	GND		
A9	Ln6p-1	B9	Ln7p-1
A10	Ln6n-1	B10	Ln7n-1
		B11	GND

TABLE 4.19: x4 (One Bi-Directional) 8 Channel PCIe Pinout

Pin #	Signal Name	Pin #	Signal Name
		B1	GND
A1	Ln0p-D1	B2	Ln0p-U1
A2	Ln0n-D1	B3	Ln0n-U1
A3	GND		
A4	Ln1p-D1	B4	Ln1p-U1
A5	Ln1n-D1	B5	Ln1n-U1
		B6	GND
A6	Ln2p-D1	B7	Ln2p-U1
A7	Ln2n-D1	B8	Ln2n-U1
A8	GND		
A9	Ln3p-D1	B9	Ln3p-U1
A10	Ln3n-D1	B10	Ln3n-U1
		B11	GND

TABLE 4.20: x4 (Two Uni-Directional) Specific 8 Channel PCIe Pinout

Pin #	Signal Name	Pin #	Signal Name
		B1	GND
A1	Ln1p-1	B2	Ln0p-1
A2	Ln1n-1	B3	Ln0n-1
A3	GND		
A4	Ln2p-1	B4	Ln3p-1
A5	Ln2n-1	B5	Ln3n-1
		B6	GND
A6	Ln1p-2	B7	Ln0p-2
A7	Ln1n-2	B8	Ln0n-2
A8	GND		
A9	Ln2p-2	B9	Ln3p-2
A10	Ln2n-2	B10	Ln3n-2
		B11	GND

TABLE 4.21: x2 (Two Bi-Directional) Specific 8 Channel PCIe Pinout

Pin #	Signal Name	Pin #	Signal Name
		B1	GND
A1	Ln0p-D1	B2	Ln0p-U1
A2	Ln0n-D1	B3	Ln0n-U1
A3	GND		
A4	Ln1p-D1	B4	Ln1p-U1
A5	Ln1n-D1	B5	Ln1n-U1
		B6	GND
A6	Ln0p-D2	B7	Ln0p-U2
A7	Ln0n-D2	B8	Ln0n-U2
A8	GND		
A9	Ln1p-D2	B9	Ln1p-U2
A10	Ln1n-D2	B10	Ln1n-U2
		B11	GND

TABLE 4.22: x1 (Two Bi-Directional) Specific 8 Channel PCIe Pinout

Pin #	Signal Name	Pin #	Signal Name
		B1	GND
A1	Ln0p-D1	B2	Ln0p-U1
A2	Ln0n-D1	B3	Ln0n-U1
A3	GND		
A4	NC	B4	NC
A5	NC	B5	NC
		B6	GND
A6	Ln0p-D2	B7	Ln0p-U2
A7	Ln0n-D2	B8	Ln0n-U2
A8	GND		
A9	NC	B9	NC
A10	NC	B10	NC
		B11	GND

TABLE 4.23: x1 (Four Bi-Directional) Specific 8 Channel PCIe Pinout

Pin #	Signal Name	Pin #	Signal Name
		B1	GND
A1	Ln0p-D1	B2	Ln0p-U1
A2	Ln0n-D1	B3	Ln0n-U1
A3	GND		
A4	Ln0p-D2	B4	Ln0p-U2
A5	Ln0n-D2	B5	Ln0n-U2
		B6	GND
A6	Ln0p-D3	B7	Ln0p-U3
A7	Ln0n-D3	B8	Ln0n-U3
A8	GND		
A9	Ln0p-D4	B9	Ln0p-U4
A10	Ln0n-D4	B10	Ln0n-U4
		B11	GND

Chapter 5

Installation

To install the Mid-Bus Probe follow the steps below:

5.1 Installation Steps for Mid-Bus Probe Pod and Related Components

1. Install probe connector into PCI Express target system board.

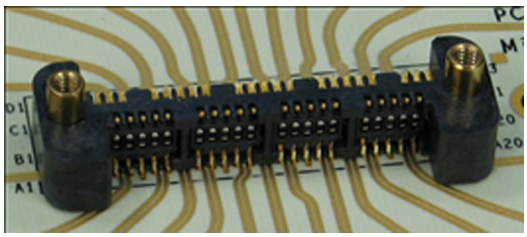


Figure 5.1: Full Width Connector for a Mid-Bus Probe

The probe connector allows the Teledyne LeCroy mid-bus probe to attach to the target system board. The probe connector is installed by aligning the module pins with the holes on the target system board. The probe connector is keyed - so be sure to orient it so that it matches the connector.

2. Bolt the probe connector to the board.
3. Plug the mid-bus probe header into the probe connector as shown below.



Figure 5.2: Cable Connection to PCB Connector

4. Carefully tighten the probe to the target by using the two thumbscrews. The thumbscrews should be screwed in only finger-tight.

Caution: The probe is delicate equipment. Please tighten the thumbscrew carefully while watching the LEDs on the probe pod. Over-tightening the probe header might damage the miniature probing spring pins.

5. Connect the four probe cables to the mid-bus probe pod ports marked **A[0-3]**, **B[0-3]**, **A[4-7]** and **B[4-7]**, using the labels on the cables to match each cable to the correct connector on the pod. The mid-bus probe pod amplifies the signal and sends it to the analyzer. The PCIe 3.0 (Gen3) probe pod is shown below.

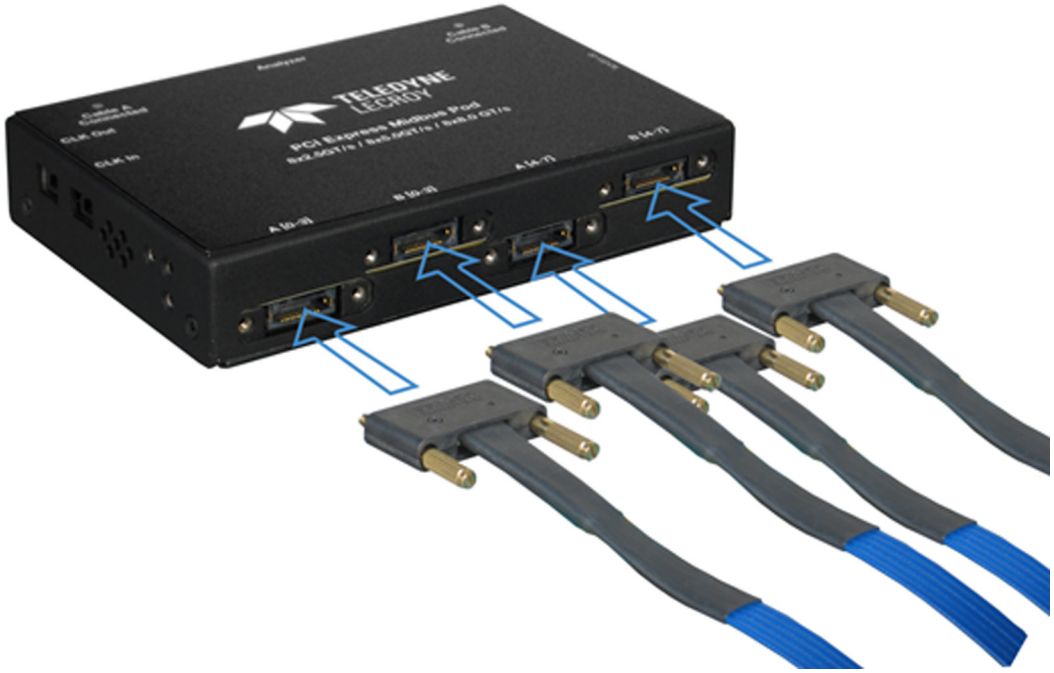


Figure 5.3: Mid-Bus Probe Pod and Associated Cables to DUT

6. If you intend to use the analyzer's reference clock, connect the three pin clock cable to the port marked "Clk In" (Reference Clock In) on the mid-bus probe pod.
7. Connect the other end of the clock cable to the three-pin reference clock header on the PCI Express board. Orientation of the cable does not matter.
8. Connect the single-headed end of the Y-cable to the pod port marked "Analyzer." See figure on next page.



Figure 5.4: Mid-Bus Probe Pod with Cable to Analyzer

9. Connect the other ends of the cable to the analyzer as follows: The "A" side of the cable plugs into the **Upstream 0-7** and the "B" side of the cable plugs into the **Downstream 0-7** ports on the Summit Analyzer. If using two Gen3 Probe pods for x16 applications on a Summit T3-16 Analyzer, connect the second probe pod using the **Upstream 8-16** and **Downstream 8-16** ports on the Summit T3-16 Analyzer. When using a Summit T34 Analyzer just connect the straight cable between the pod and the analyzer.

5.2 Reference Clock Cable

The Reference Clock Cable (PE014UCA-X) connects the Mid-Bus Pod to the DUT so that the pod can use the clock from the DUT. The cable has a 3-pin micro socket at one end that attaches to a 3-pin header (0.050" spacing) designed into the DUT, and the other end connects to the Clk In port on the Mid-Bus Probe Pod, as shown below.

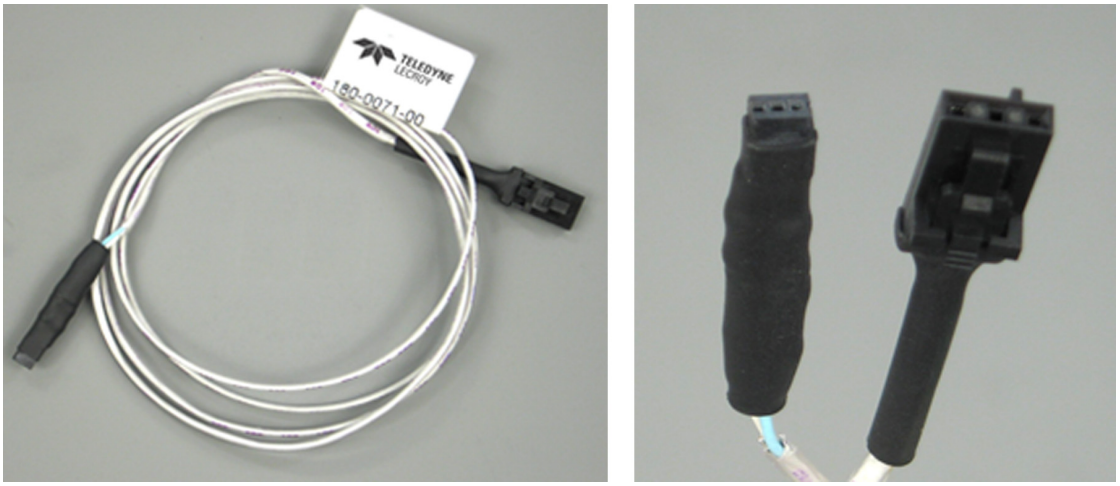


Figure 5.5: Reference Clock Cable

5.3 Daisy-Chain Cable

The Daisy Chain Cable (PE009UCA-X) connects multiple Mid-Bus Pods together so they can share the same clock. One end of the connector is attached to the **Clk Out** port of the Mid-Bus Pod supplying the clock signal, and the other end is connected to the **Clk In** port of the other Mid-Bus Pod, as shown below.





Chapter 6

Dual Probe Pod Setup Using External Clocking

The steps outlined above in Chapter 5, “Installation,” on page 37 describe a single Probe/ single Analyzer configuration. In a dual analyzer setup, a second probe may need to be added depending on the type of link that is being recorded.

If the analyzer internal clock is to be used, then cable the target device to the probe pod as follows - however, omit the 3-pin reference clock cable(s) shown in the illustration.

If external clocking is to be used, using the PE014UCA-X Ref Clock cable, connect the 3-pin reference clock cable from the 3-pin header on the system board to the **CLK IN** port on one probe pod. Then using the PE009UCA-X Daisy Chain Cable, connect the **CLK OUT** port on that same pod and connect it to the **CLK IN** port on the second pod. The setup is shown below.

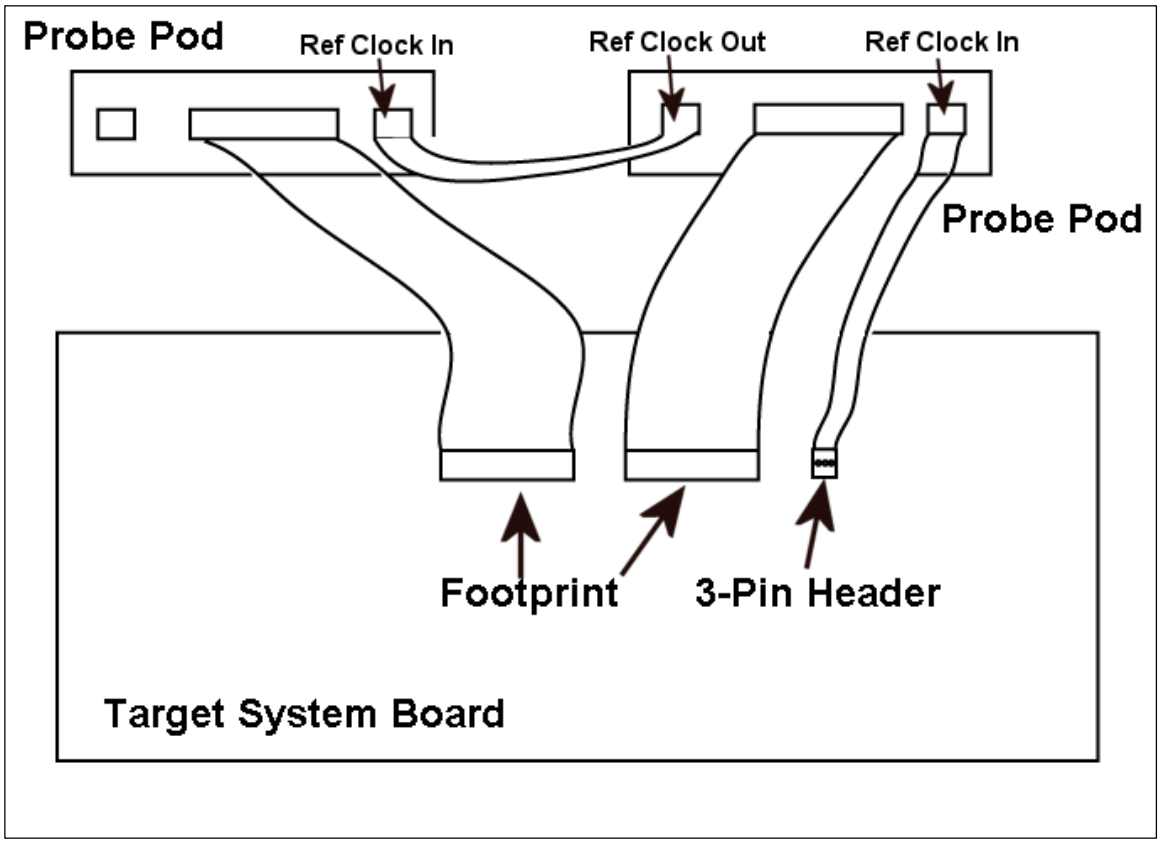


Figure 6.1: Dual Probe Pod Configuration

Chapter 7

Recording Traffic

For instructions on setting up and implementing a recording, please refer to the user manual for the Teledyne LeCroy protocol analyzer being used.

Chapter 8

Ordering Information

Use the following table of part numbers and descriptions to order components for Teledyne LeCroy PCIe 3.0 Mid-bus probes. Ordering Information Table 8.1, “Ordering Information -- Analyzers and Probes,” on page 48 and Table 8.2, “Ordering Information - Cables and Accessories,” on page 49.

TABLE 8.1: Ordering Information -- Analyzers and Probes

Gen3 Analyzers	
PE050AAA-X	Summit T3-16 (licensed as a Gen3 x16 analyzer, no probes or cables)
PE051AAA-X	Summit T3-16 (licensed as a Gen3 x8 analyzer, no probes or cables)
PE060AAA-X	Summit T3-8 (licensed as a Gen3 x8 analyzer, no probes or cables)
PE061AAA-X	Summit T3-8 (licensed as a Gen3 x4 analyzer, no probes or cables)
PE062AAA-X	Summit T3-8 (licensed as a Gen3 x1 analyzer, no probes or cables)
PE080AAA-X	Summit T34 (licensed as a Gen3 x4 analyzer, no probes or cables)
PE081AAA-X	Summit T34 (licensed as a Gen3 x1 analyzer, no probes or cables)
Gen3 Mid-Bus Probes	
PE087ACA-X	PCIe3 Mid-bus Pod with Thumbscrews, no cables (for use with Summit T3-16, Summit T3-8 or Summit T34), includes power supply.
PE090ACA-X	PCIe3 Full-size Mid-bus Probe Kit [includes Mid-bus pod with Thumbscrews, iPass Y-cable, power supply, G3x8 Probe Cable, Full-size Probe Connector, Ref Clock Cable and Daisy Chain Clock Cable (for connecting two pods to support bi-directional x8)]. Supports up to bi-directional x8 link or uni-directional x16 link (for use with Summit T3-8 or T3-16).
PE091ACA-x	PCIe3 Half Size Mid-bus Probe Kit [includes Mid-bus pod with Thumbscrews, iPass Straight Cable, power supply, G3x4 Probe Cable, Half-size Probe Connector, two (2)Ref Clock Cables and two (2) Daisy Chain Clock Cables (to connect two pods to support bi-directional x8)]. Supports up to Bi-directional x4 link or Uni-directional x8 link. For use with Summit T34 systems only.
PE094ACA-X	PCIe3 Half-size Mid-bus Probe Kit [includes Mid-bus pod with Thumbscrews, iPass Y-Cable, power supply, G3x4 Probe Cable, Half-size Probe Connector, Ref Clock Cable and Daisy Chain Clock Cable (to connect two pods to support bi-directional x8)]. Supports up to bi-directional x4 link or uni-directional x8 link (for use with Summit T3-8, SummitT3-16 or dual Summit T34).
PE056ACA-X	PCIe3 Mid-bus Probe Cable with Thumbscrews, G3x4 probe cable (Half size -- connects to G3 Mid-bus box, for use with Summit T3-16, Summit T3-8 or Summit T34).
PE057ACA-X	PCIe3 Mid-bus Probe Cable with Thumbscrews, G3x8 probe cable (Full size -- connects to G3 Mid-bus box, for use with Summit T3-16, Summit T3-8 or Summit T34).

TABLE 8.2: Ordering Information - Cables and Accessories

Cables and Accessories	
PE010UCA-X	iPass Y-Cable (for use with Summit T2-16, T28, T3-8, T3-16 or dual T34), 1 meter
PE009UCA-X	Daisy Chain Cable (for use with x4 Multi-lead Pod and Mid-bus Pod)
PE014UCA-X	Reference Clock Cable (for use with x4 Multi-lead Pod and Mid-bus Pod)
PE038UIA-X	PCIe Gen3 Dish for Mid-bus Probe
PE047UIA-X	Gen3 Mid-Bus Probe Connector Full-Size
PE054UIA-X	Gen3 Mid-Bus Probe Connector Half-Size
PE013UCA-X	x4-tox8 Straight iPass Cable (for use with Summit T24, T2-16, T28, T34, T3-8, T3-16 or Eclipse X34), 1 meter

Chapter 9

Updates and Licensing

9.1 Updating the Analyzer

BusEngine™ and/or Firmware updates are now automatic processes that run anytime a new version of the PCIe Protocol Suite™ software is installed that is incompatible with the currently installed BusEngine or Firmware. The update process generates onscreen instructions.

If, however, you need to manually perform BusEngine or Firmware updates, follow these steps:

1. Select **Setup > Update Device** … from the menu to display the Update Analyzer dialog box for **Summit T3-16™.**
2. Select the appropriate file locations for the Firmware and/or BusEngine, using Browse, if necessary.
3. Check the appropriate options (if in doubt, check all options).
4. Click **Update** to initiate the updating of the Analyzer.

9.2 License Keys

A License Key is necessary to enable software maintenance. If you attempt to record with the Analyzer without an installed License Key, a message appears to indicate that a License Key is necessary in order to record traffic.

A License Key must be obtained from Teledyne LeCroy for each Analyzer.

After you obtain the License Key, follow these steps to install it:

1. Select **Setup > All Connected Devices > Update License** from the menu bar. to display the Select License Key File dialog box.
2. Enter the **path** and **filename** for the License Key or use the Browse button to navigate to the directory that contains the License Key.
3. Select the **.lic** file, and then click **Update Device**.

9.3 License Information

You can view Licensing information for your Analyzer by selecting **Help > Display License Information**... from the menu bar. The License Information window displays data about the maintenance expiration and purchased features.

Appendix A

How to Contact Teledyne LeCroy

Send e-mail to Support	psgsupport@teledyne.com
Contact support	teledynelecroy.com/support/contact
Visit Teledyne LeCroy's web site	teledynelecroy.com
Tell Teledyne LeCroy	Report a problem to Teledyne LeCroy Support via e-mail by selecting **Help > Tell Teledyne LeCroy** from the application toolbar. This requires that an e-mail client be installed and configured on the host machine.

Appendix B

China Restriction of Hazardous Substances Table

The following tables are supplied in compliance with China's Restriction of Hazardous Substances (China RoHS) requirements:

	有毒有害物质和元素					
部件名称	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr^{6+})	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
PCBAs	X	O	X	X	X	X
机械硬件	O	O	X	O	O	O
金属片	O	O	X	O	O	O
塑料部件	O	O	O	O	X	X
电源	X	X	X	O	X	X
电源线	X	O	X	O	X	X
保护外壳(如有)	O	O	O	O	X	X
电缆组件(如有)	X	O	X	O	X	X
风扇(如有)	X	O	X	O	X	X
交流滤波器和熔丝组件(如有)	X	O	X	O	O	O
外部电源(如有)	X	X	X	O	X	X
探头(如有)	X	O	X	O	X	X
O: 表明该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T11363-2006 标准规定的限量要求之下。						
X: 表明该有毒有害物质至少在该部件的某一均质材料中的含量超过 SJ/T11363-2006 标准规定的限量要求。						

EFUP (对环境友好的使用时间) 使用条件:
温度: 5摄氏度到40摄氏度
湿度: 5% - 95%最大相对湿度 (无冷凝)
高度: 最高2000米

	Toxic or Hazardous Substances and Elements					
Part Name	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr^{6+})	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
PCBAs	X	O	X	X	X	X
Mechanical Hardware	O	O	X	O	O	O
Sheet Metal	O	O	X	O	O	O
Plastic Parts	O	O	O	O	X	X
Power Supply	X	X	X	O	X	X
Power Cord	X	O	X	O	X	X
Protective Case (if present)	O	O	O	O	X	X
Cable Assemblies (if present)	X	O	X	O	X	X
Fans (if present)	X	O	X	O	X	X
AC Filter/Fuse Assy (if present)	X	O	X	O	O	O
Ext Power Supply (if present)	X	X	X	O	X	X
Probes (if present)	X	O	X	O	X	X
O: Indicates that this toxic or hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement specified in SJ/T11363-2006.						
X: Indicates that this toxic or hazardous substance contained in at least one of the homogenous materials used for this part is above the limit requirement specified in SJ/T11363-2006.						

EFUP (Environmental Friendly Use Period) Use Conditions:

Temperature	5C to 40C
Humidity	5% to 95% max RH (non-condensing)
Altitude	Up to 2000 meters

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